IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner: James M. Mitchell
Art Unit: 2827

In Re PATENT APPLICATION Of:

Applicant : Shinji OHUCHI et al.

Applic. No. : 09/843,650

Filed : April 27, 2001

For SEMICONDUCTOR APPARATUS APPARATUS AND METHOD FOR FABRICATING THE SAME

Attorney Ref.: IIZ 123

SUPPLEMENTAL RESPONSE

October 8, 2002

Commissioner for Patents
Washington, D.C. 20231

Sir:

Further to the Amendment filed October 3, 2002 in response to the Examiner's Action dated July 3, 2002, submitted herewith are clean and marked-up versions of the amended claims 1 - 3, 7, 9, 11, 13 - 15, 17, and 19.

AMENDED CLAIMS

1. (Amended) A semiconductor apparatus comprising:

a semiconductor device to be mounted on a circuit board;

a plurality of conductive posts electrically connected to the semiconductor device; and

means for mounting the device onto a circuit board by soldering, including a plurality of conductive bumps respectively positioned on an outer end of each of the conductive posts for soldering onto the circuit board, wherein a peripheral edge of a resin covering for sealing a surface of the semiconductor device and an outer edge of the conductive post are separated by a distance narrower than a height of the conductive post.

2. (Amended) A semiconductor apparatus according to claim 1, wherein the distance is in a range between 50 and 100 micrometers.

3. (Amended) A semiconductor apparatus according to claim 1, wherein the semiconductor device is provided with a plurality of electrode pads connected to the conductive posts, the electrode pads being arranged on a line extending in a center portion of the semiconductor device.

7. (Amended) A semiconductor apparatus comprising:

a semiconductor device;

a plurality of conductive posts electrically connected to the semiconductor device;

means for mounting the device onto a circuit board by soldering, including a plurality of conductive bumps respectively positioned on an outer end of each of the conductive posts for soldering onto the circuit board; and

a molding resin covering a surface of the semiconductor device, wherein the molding resin is shaped to have a step along the entirety of a peripheral edge of the semiconductor device, the step having upper and lower level portions.

9. (Amended) A semiconductor apparatus according to claim 7, wherein the difference in level between the upper portion and lower portion of the step is in a range between 40 and 60 micrometers.

11. (Amended) A semiconductor apparatus comprising:

a semiconductor device;

a plurality of conductive posts electrically connected to the semiconductor device;

means for mounting the device onto a circuit board by soldering, including a plurality of first conductive bumps respectively positioned on an outer end of each of the conductive posts for soldering onto the circuit board;

a molding resin covering a surface of the semiconductor device without covering a peripheral side surface of the conductive posts; and

an insulating layer formed on a peripheral surface of the semiconductor device between an upper surface of the semiconductor device and the conductive posts, wherein the molding resin is shaped to have a peripheral side surface on the identical plane with the peripheral side surface of the semiconductor device.

13. (Amended) A semiconductor apparatus according to claim 11, further comprising

a plurality of second conductive bumps each provided on a respective peripheral side surface of a respective one of the conductive posts.

14. (Amended) A semiconductor apparatus according to claim 11, wherein the first conductive bumps are of solder.

15. (Amended) A method for fabricating a semiconductor apparatus according to claim 7, comprising the steps of:

providing a semiconductor wafer on which a plurality of semiconductor devices are formed, each of the semiconductor device having electrode pads thereon;

providing a plurality of conductive post connected to the electrode pads of the semiconductor devices;

molding the semiconductor devices with a molding resin so that an upper surface of the molding resin is on the same plane with upper surfaces of the conductive posts;

removing a part of the molding resin to be located at a peripheral edge so that the peripheral edge of the molding resin has a step, the step having upper and lower level portions;

providing conductive bumps on outer ends of the conductive posts; and

dicing the semiconductor wafer to form a plurality of individual semiconductor apparatuses.

17. (Amended) A method according to claim 15, wherein the difference in level between the upper portion and lower portion of the step is in a range between 40 and 60 micrometers.

19. (Amended) A method for fabricating a semiconductor apparatus according to claim 11, comprising the steps of:

providing a semiconductor wafer on which a plurality of semiconductor devices are formed, each of the semiconductor devices having electrode pads thereon;

forming grooves in the semiconductor wafer at portions corresponding to dicing lines of the semiconductor wafer;

forming an insulating layer on the wafer so that the grooves are filled with the insulating layer but a part of each electrode pad of the semiconductor devices is not covered with the insulating layer;

forming a metal layer on the insulating layer and the part of each electrode pad, not covered with the insulating layer;

forming a rewiring layer on the metal layer;

providing a conductive post material extending across each of the grooves;

molding the semiconductor wafer with a molding resin so that an upper surface of the molding resin is on the same plane with upper surfaces of the conductive post material across each of the grooves;

providing a conductive bump material on the conductive post material; and

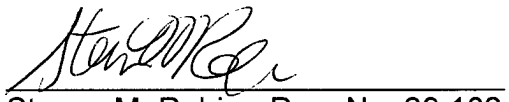
dicing the semiconductor wafer at the grooves to form a plurality of individual semiconductor apparatuses.

REMARKS

Clean and marked-up copies of the amended claims are submitted because in the Amendment filed October 3, 2002, only marked-up claims were provided.

Should the Examiner feel that a further conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,



October 8, 2002
Date

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